SPECIFICATION AMENDMENTS

Please replace the BACKGROUND OF THE INVENTION section beginning on page 1, line 9, with the following rewritten section:

BACKGROUND OF THE INVENTION

1. ~~Technical Field~~ Technical Field of the Invention

This disclosure generally relates to methods of fabricating semiconductor devices and more specifically to methods of fabricating silicide layers that are aligned to source/drain regions.

2. ~~Detailed Description of the Invention~~ Description of the Related Art

A conventional method for fabricating a semiconductor device is to form a silicide layer on source/drain regions and on a polysilicon gate. The silicide layer provides various advantages such as a good ohmic contact, lowering the resistance of the polysilicon gate, and providing an etch stop layer to the source/drain region and the polysilicon gate.

A conventional process for forming a silicide layer is a self-aligned silicide process, also known as a salicide process. The salicide process includes a step of forming a metal layer, for instance, formed of cobalt, nickel or titanium combining silicon without reacting with a silicon oxide layer and a silicon nitride layer. The metals react with the silicon to form a low-resistance silicide such as $CoSi_2$, NiSi or $TiSi_2$. The salicide process is applied to the semiconductor substrate with a gate electrode and source/drain region to form an aligned silicide layer on the source/drain regions and on the gate electrode with exposed silicon. The salicide process may form a thin and uniform silicide layer on the source/drain region and on the gate electrode.

In processes for fabricating semiconductor devices, a trench isolation layer is used for electrically isolating unit elements adjacent to each other. However, the trench isolation layer has a disadvantage that a dent is formed on a boundary with the active region.

Figs. 1 and 2 are cross-sectional diagrams illustrating a conventional method for fabricating semiconductor devices.

Referring to Fig. 1, an isolation layer 12 is formed in a semiconductor substrate 10 to define an active region 14 by a trench isolation technique. As shown in Fig. 1, it is common for a dent to form in the isolation layer 12 neighboring the active region 14.

Referring to Fig. 2, a gate pattern 16 is formed on the active region 14, and source/drain regions 18 are formed in the active region neighboring the gate electrode 16.

Sidewall spacers 20 are formed on sidewalls of the gate electrode 16. Continuously, a conventional salicide process is applied to the resultant structure to form a silicide layer 22 on the source/drain regions 18 and the gate pattern 16. Because a dent D exists on a boundary between the active region 14 and the isolation layer 12, the silicide layer 22 is formed along a topology of the dent because the silicide layer provided by the salicide process is thin and uniform. Therefore, the silicide layer 22 forms a deep spike 26 to a bottom of the substrate in the dent D. As a result, leakage current occurs due to a focusing of electrical field through the spike 26, making the resulting shallow source/drain structure ineffective for preventing short channel effects such as punch through.

Embodiments of the invention address these and other disadvantages of the prior art.

Please replace the paragraph beginning on page 3, line 20, with the following rewritten paragraph:

A gate pattern 56 is formed on the active region 54. The gate pattern 56 crosses over the active region 54 and the isolation layer 52 (not shown). Source/drain regions 58 are formed in the active region 54 to both sides of the gate patterns 56. A spacer insulation layer 60 is formed on a semiconductor substrate 50 with the gate pattern 56. The spacer insulation layer 60 may be formed of silicon oxide or silicon nitride.